REMARKS

Claims 1-10 were examined in the March 10, 2009 Final Office Action. Claims 1-2 and 5-7 are objected to for informalities. Claims 1-10 stand rejected as obvious over FIG. 1, admitted prior art, in view of U.S. Patent No. 4,499,388 to *Adam* in view of U.S. Patent No. 4,926,423 to *Zukowski*. Reconsideration of these objections and rejections is requested in view of the above claim amendments and following remarks.

A. Objection of Claims 1-2 and 5-7 is Addressed.

Claims 1-2 and 5-7 are objected to for variations references to the four-terminal inverter as the or said inverter. Claims 1 and 6 have been amended as suggested by the Examiner, to remove mention of "four-terminal" and recite only "an", "the" or "said" inverter. Withdrawal of the objection of claims 1-2 and 5-7 is respectfully requested.

B. Obviousness Rejection of Claims 1-10 is Addressed.

The rejection of claims 1-10 under 35 U.S.C. § 103(a) over admitted prior art (FIG. 1) in view of U.S. Patent No. 4,499,388 to *Adam* and U.S. Patent No. 4,926,423 to *Zukowski* is respectfully traversed.

As previously argued, *Adam* in combination with the admitted prior art cannot be said to suggest the claimed "inverter" of the present invention wherein each of the four inverter circuit nodes are separate as claimed. This is acknowledged in the final Office Action at page 4, lines 13-15.

1. *Zukowski*'s Field Of Endeavor Is Improperly Characterized And *Zukowski* Constitutes Non-Analogous Art, And With *Zukowski*, *Prima Facie* Obviousness Of Claims 1-10 Is Not Established

The Office Action turns to *Zukowski*, asserting that it is in the same field of endeavor, i.e., "logic controlled selection circuits". However, the field of the endeavor is stated at col. 1, lines 6-13 of *Zukowski* to actually relate to

> . . . . high-speed serial data transmission systems, and more particularly to a serial high-speed data transmission system which uses time-division multiplexing and demultiplexing techniques in which the maximum permissible data transmission rate of the system is not limited by the switching speed or settling time of latches used in the multiplexer and demultiplexer circuits . . . .

The Examiner's characterization of the *Zukowski*'s field of the endeavor is arbitrary and unduly broad.

Applicant's field of endeavor is "a system for driving rows of a liquid crystal display." Clearly the fields of endeavour of the present application and of *Zukowski* are different.

MPEP 2141.01(a) summarizes how "In order to rely on a reference as a basis for rejection of an applicant's invention, the reference must either be in the field of applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the inventor was concerned." *In re Oetiker*, 977 F.2d 1443 (Fed. Cir. 1992). "A reference is reasonably pertinent if, even though it may be in a different field from that of the inventor's endeavor, it is one which, because of the matter with which it deals, logically would have commended itself to an inventor's attention in considering his problem." *Wang Labs. Inc. v. Toshiba Corp.*, 993 F.2d 858 (Fed. Cir. 1993).

The matter with which the present invention deals involves is "in planning the driving devices of LCD rows and columns is to reduce the power consumption so as to minimize both the power delivered by the power supplies of said devices, and the power dissipated by them." *See* the present specification "Background of the Invention". The matter with which *Zukowski* deals is "a need for a time-division multiplexed data transmission system that avoids the limitations imposed by slow switching and settling times of latches and other logical componetnts, and avoids the problem of having to generate and distribute a clock signal of a frequency as great s the output data rate of the multiplexer." *See* col. 4, lines 3-9.

Clearly, the problem to which *Zukowski* is directed would not logically have commended itself to the attention of the inventors' hereof, in considering the problem in which they were dealing. Thus, applying the Federal Circuit law consistently with MPEP 2141.01(a), *Zukowski* does not constitute analogous art and cannot be relied on to support the rejection of claims 1-10. *Prima facie* obviousness having not been established with the admitted prior art and *Adam* alone, withdrawal of the obviousness rejection of claims 1-10 is proper and respectfully requested.

2. *Zukowski* Teaches A Multiplexer Circuit, Not The Claimed Inverter Circuit, So That The Combination Of Admitted Prior Art, *Adam* And *Zukowski* Fail To Teach Or Suggest All Of The Claimed Elements, So That *Prima Facie* Obviousness Of Claims 1-10 Is Not Established

Zukowski teaches a multiplexer circuit, not the claimed inverter circuit. The Examiner minimizes this literal difference by saying that the multiplexer circuit merely has a "different internal structure" with the same logic function. This conclusion is incorrect and respectfully traversed. A multiplexer circuit does not have the same logic function as the claimed inverter circuit. Moreover, the claims are claiming an actual inverter where the power supply terminals are literally power supply terminals for providing energy to the circuit and are not part of the logic function. There is no multiplexing through the recited power terminals.

More particularly, an inverter is a four terminal device, having an input, an output, a first power terminal and a second power terminal. The logic function of an inverter is set forth in the table below. In an inverter, there is only one logic function. The output is the inverse of the input. The output signal will, however, be influenced by the voltage level of the first and second power terminals. For example, if the first power terminal is set to VDD, then the output signal when the output is high will be approximately VDD minus any voltage drop caused by the design of the inverter. Similarly, if the second power terminal is set to VSS, then the output signal when the output is low will be approximately VSS plus any voltage drop caused by the design of the inverter.

INPUT	OUTPUT
0	1
1	0

Inverter Logic Function

In contradistinction, as known by those of ordinary skill in the art, a multiplexer is a six terminal device, having two logic inputs, an output, a select input, a first power terminal and a second power terminal. The logic function of a multiplexer is that, in a first logic state of the select input a first logic input is selected to be transferred to the output, and, in a second logic state of the select input a second logic input is selected to be transferred to the output. The level of the output signal will again be influenced by the voltages on the first and second power terminals. The logic function of a multiplexer is set forth in the table below.

A INPUT	B INPUT	SELECT INPUT	OUTPUT
A (0 or 1)	B (0 or 1)	0	A (0 or 1)
A (0 or 1)	B (0 or 1)	1	B (0 or 1)

Multiplexer Logic Function

The differences between an inverter and a multiplexer are deemed to be clear and well known by those of ordinary skill in the art. The claims claim a bona fide inverter in conjunction with two switches for driving a row in a liquid crystal display. The claimed inverter is an inverter and not a multiplexer. In the manner framed by the Examiner, i.e. an inverter is a multiplexer, the Applicants cannot agree and point to the obvious differences between the two.

Further, the inverter of the present invention is not altered beyond its normal operating mode wherein the power terminals themselves are deemed to be logic inputs, if this is what is being implied by the Examiner's argument. The claimed inverter works in the normal manner of operation, wherein the power terminals are power terminals for receiving energy for operating the circuit, although the inverter is acted upon by other elements in the claim. The claimed inverter does not use the power terminals as logic inputs, wherein the first power terminal can be toggled between a logic one and a logic zero, or wherein the second power terminal can be toggled between a logic one and a logic zero.

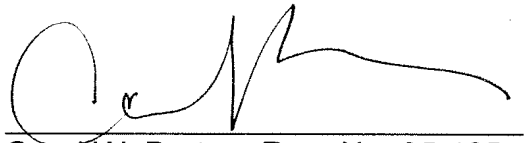
In view of these differences, the claims now pending clearly recite features not taught by *Zukowski* and clearly distinguish over *Zukowsky* in combination with admitted prior art and *Adam*. For these further reasons, even if one were to improperly rely on *Zukowsky,* despite the precedence of federal patent law as established by the Court of Appeals for the Federal Circuit under which *Zukowsky* constitutes non-analogous art, claims 1-10 are non-obvious and patentable over the cited combination. Withdrawal of the obviousness rejection of claims 1-10 is therefore proper and respectfully requested.

C. Conclusion.

Pending claims 1-10 all being in form for allowance, such action is respectfully requested. Should any issues remain, the Examiner is kindly asked to telephone the undersigned.

Although no fee is believed to be due, the Office is authorized to charge Deposit Account No. 50-1123 any fee deficiencies associated with this filing.

Respectfully submitted,



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